REMARKS

Claims 32, 55, 68 and 97 have been amended. Claim 98 has been added. Claims 66-67 have been canceled. Claims 32-55, 57-65, 68 and 97-98 are now pending. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the above-referenced application in light of the amendments and following remarks.

Claim 97 stands rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The rejection is respectfully traversed. The Office Action asserts that the claim language reciting the top electrode comprising 'a bottom and top conducting layer' is not described in the original specification. Applicants respectfully disagree; but, nonetheless, to expedite prosecution, claim 97 has been amended to omit this claim language. Consequently, the § 112, first paragraph rejection should be withdrawn.

Claims 55 and 68 stand objected to because of informalities. In accordance with the Office Action's recommendations, claims 55 and 68 have been amended. Consequently, the objections should now be withdrawn.

Claims 32-36, 40-45, 47-49, 51-52, 54, 57-58 and 62-63 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,338,996 ("Iizuka"). The rejection is respectfully traversed.

The cited reference fails to teach the subject matter of amended independent claim 32. Specifically, Iizuka does not disclose a method of forming a capacitor comprising, *inter alia*, "forming a bottom conducting layer . . . forming a dielectric layer, and annealing said dielectric layer with *a first anneal process* . . . forming a top electrode with a top conducting layer . . . and annealing the top electrode with *a second anneal*

process using an oxidizing gas anneal, said oxidizing gas anneal performed *between 10 seconds to about 30 minutes*," as recited in claim 32 (emphasis added).

In FIG. 1, Iiuzuka discloses a capacitor 20 consisting of a lower electrode 28, a capacitance film 30, and an upper electrode 32. In the first embodiment, Iizuka teaches that "*[a]fter* forming the high dielectric thin film capacitor, [an] anneal is performed for about 40 minutes under a normal pressure in a nitrogen atmosphere at temperature of 300 to 400 degrees C." (Col. 4, ll. 28-31) (emphasis added). In the second embodiment, Iizuka discloses that "*[a]fter* the high dielectric thin film capacitor is formed, [an] anneal is performed in a gas mixture of oxygen (5% or below) and nitrogen at a temperature of 300 to 400 degrees C. for about 40 minutes." (Col. 4, ll. 55-59) (emphasis added).

Iizuka does not disclose that the dielectric layer itself undergoes a *first anneal process* and then the top conducting layer undergoes a *second anneal process* with an oxidizing gas anneal. At best, Iizuka merely teaches a single anneal process for the entire structure. Iizuka does not teach that the dielectric layer and top conducting layer undergo *separate* anneal processes. This is an important aspect of Applicants' claimed invention.

The "present invention further improves the dielectric property of the dielectric layer 36 by *adding* an oxidizing gas anneal (second anneal) which *fills* the oxygen voids created in the dielectric layer *after* the top conducting layer 38 is deposited." (Applicants' specification, p. 8, ll. 8-10) (emphasis added). A first anneal is conducted on the dielectric layer to improve the dielectric property and a second anneal is conducted to fill in oxygen voids after the top conducting layer is deposited. Iizuka does not disclose such a process.

Moreover, in both embodiments, Iizuka teaches that in the nitrogen atmosphere-containing *and* the oxygen plus nitrogen atmosphere-containing anneals, the duration of *both* anneals is about *40 minutes*. The present invention, in contrast, indicates that the dielectric property is improved with an oxidizing gas anneal which fills oxygen voids with a duration of 10 seconds to 30 minutes (Applicants' specification, p. 8, ll. 8-13). Iizuka does *not* disclose an "oxidizing gas anneal performed *between 10 seconds to about 30 minutes*," as recited in claim 32 (emphasis added). Iizuka's claimed process is at least 33% longer in duration than Applicants' claimed process.

Claims 33-36, 40-45, 47-49, 51-52, 54, 57-58, and 62-63 depend from claim 32 and should be similarly allowable along with claim 32 for at least the reasons provided above regarding claim 32, and on their own merits.

For example, Iizuka does *not* teach that the "dielectric layer is an amorphous dielectric layer which is heated to a temperature above 200 degrees Celsius to change said dielectric layer from an amorphous to a crystalline material," as recited in dependent claim 47. The Office Action asserts that Iizuka's Col. 4, ll. 55-63 teaches the claimed method. This is not true.

In Iizuka, col. 4, ll. 55-60, discloses the "semiconductor memory device production method according to a *second embodiment* of the present invention." (emphasis added). In the second embodiment, Iizuka discloses that a gas mixture of oxygen (5% or below) *and* nitrogen can be used (Col. 4, ll. 55-59). Iizuka does *not* disclose any method of separately heating or annealing a dielectric layer. This is an additional reason for the allowance of dependent claim 47.

Claims 37-38 and 50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh"). The rejection is respectfully traversed.

Claims 37-38 and 50 depend from claim 32 and should be similarly allowable with claim 32 for at least the reasons provided above with regard to claim 32, and on their own merits. Specifically, Iizuka does *not* disclose or suggest "annealing [a] dielectric layer with *a first anneal process* . . . forming a top electrode with a top conducting layer . . . and annealing the top electrode with *a second anneal process* using an oxidizing gas anneal, said oxidizing gas anneal performed *between 10 seconds to about 30 minutes*," as recited in claim 32 (emphasis added). Iizuka does not disclose, in either the first or second embodiment, a first and second anneal process or an anneal duration that is between 10 seconds to about 30 minutes.

With respect to dependent claims 37, 38 and 50, the Office Action acknowledges that Iizuka does not disclose a bottom conducting layer that is a metal alloy or conducting metal oxide, or that the top conducting layer is a conducting metal oxide (p. 6). In view of Iizuka's shortcomings, the Office Action relies on Emesh for this disclosure and summarily concludes that it would be obvious to substitute Emesh's electrode materials with Iizuka's to provide alternative materials to make the electrodes (p. 6). Applicants respectfully disagree.

Iizuka teaches away from the proposed combination. Iizuka discloses a "semiconductor device having a capacitor formed by a high dielectric insulation film and a *noble metal* upper electrode which are successively layered on a *noble metal* lower electrode." (Col. 2, ll. 28-31 and Col. 2, ll. 38-40) (emphasis added). Iizuka teaches that *both* electrodes in the capacitor should consist of a *noble metal*.

These facts are underscored by Iizuka's disclosure that "[t]he lower electrode 28 *and* the upper electrode 28 are formed by a *noble metal film* such as Ru, Ir, and Pt." (Col. 3, ll. 38-40) (emphasis added). Consequently, there is no motivation to use Emesh's metal alloy or conducting metal oxide for either the upper or lower electrodes in Iizuka since Iizuka teaches away from the proposed combination.

As such, the cited references are not properly combinable, and still would not disclose or suggest that the "bottom conducting layer is formed of a metal alloy," as recited in dependent claim 37, or that "the bottom conducting layer is formed of a conducting metal oxide," as recited in claim 38, or that "the top conducting layer is formed of a conducting metal oxide," as recited in claim 50.

Claims 39, 46 and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers"). The rejection is respectfully traversed.

Claims 39, 46 and 53 depend from claim 32 and should be similarly allowable with claim 32 for at least the reasons provided above with regard to claim 32, and on their own merits. Specifically, Iizuka does *not* disclose or suggest "annealing [a] dielectric layer with *a first anneal process* . . . forming a top electrode with a top conducting layer . . . and annealing the top electrode with *a second anneal process* using an oxidizing gas anneal, said oxidizing gas anneal performed *between 10 seconds to about 30 minutes*," as recited in claim 32 (emphasis added). Iizuka does not disclose, in either the first or second embodiment, a first and second anneal process or an anneal duration that is between 10 seconds to about 30 minutes.

With respect to dependent claims 39, 46 and 53, the Office Action acknowledges that Iizuka does not disclose a bottom conducting layer that is a metal nitride, or that the dielectric layer is formed of TaO and is crystalline or amorphous (p. 7). In view of Iizuka's shortcomings, the Office Action relies on Alers for this disclosure and summarily concludes that it would be obvious to substitute Alers' materials with Iizuka's to provide alternative materials to make an electrode or dielectric layer (p. 7). Applicants respectfully disagree.

As indicated above, Iizuka teaches that *both* electrodes in the capacitor should consist of a *noble metal.* Consequently, there is no motivation to combine Iizuka and Alers with regard to electrode materials since Iizuka teaches away from any other material but noble metals for the electrode. As a result, the references do not teach or suggest that the "bottom conducting layer is formed of a metal nitride," as recited in dependent claim 39.

To establish *prima facie* obviousness of a claimed invention, *all* the claim limitations must be taught or suggested *by the prior art."* M.P.E.P. § 2143.03. In this case, there is no teaching or suggestion to substitute the dielectric materials in Iizuka since the reference explicitly discloses using BST for the dielectric film (Col. 6, ll. 37-40). This is an additional reason for the allowance of dependent claim 39.

Claim 55 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of Alers and further in view of Emesh. The rejection is respectfully traversed.

Claim 55 depends from claim 32 and should be similarly allowable with claim 32 for at least the reasons provided above with regard to claim 32, and on its own merits. Specifically, Iizuka does *not* disclose or suggest "annealing [a] dielectric layer

with *a first anneal process* . . . forming a top electrode with a top conducting layer . . . and annealing the top electrode with *a second anneal process* using an oxidizing gas anneal, said oxidizing gas anneal performed *between 10 seconds to about 30 minutes,*" as recited in claim 32 (emphasis added). Iizuka does not disclose, in either the first or second embodiment, a first and second anneal process or an anneal duration that is between 10 seconds to about 30 minutes.

With respect to claim 55, the Office Action acknowledges that Iizuka does not disclose a bottom conducting layer that is tungsten nitride, or that the dielectric layer is formed of Al_2O_3. (p. 8). In view of Iizuka's shortcomings, the Office Action relies on Alers for disclosing a bottom electrode of WN and Emesh for disclosing a dielectric layer of Al_2O_3. As discussed above, there is no motivation to combine the references with Iizuka since Iizuka teaches away from the proposed combination. Iizuka teaches that both electrodes should consist of a noble metal and the dielectric layer should consist of BST.

Consequently, the references do not teach or suggest that the "bottom conducting layer is a layer of Tungsten Nitride . . . and [a] dielectric layer is a layer of Aluminum Oxide," as recited in dependent claim 55. This is an additional reason for the allowance of dependent claim 55.

Claims 59-60 and 64-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,475,854 ("Narwankar"). The rejection is respectfully traversed.

Claims 59-60 and 64-68 depend from claim 32 and should be similarly allowable with claim 32 for at least the reasons provided above with regard to claim 32, and on their own merits. Specifically, Iizuka does *not* disclose or suggest "annealing [a]

dielectric layer with *a first anneal process* . . . forming a top electrode with a top conducting layer . . . and annealing the top electrode with *a second anneal process* using an oxidizing gas anneal, said oxidizing gas anneal performed *between 10 seconds to about 30 minutes*," as recited in claim 32 (emphasis added). Iizuka does not disclose, in either the first or second embodiment, a first and second anneal process or an anneal duration that is between 10 seconds to about 30 minutes.

With respect to claims 59-60 and 64-68, the Office Action acknowledges that Iizuka does not disclose annealing at a pressure between 2-660 Torr (p. 9). In view of Iizuka's shortcomings, the Office Action relies on Narwankar for disclosing a pressure of 2-660 Torr and summarily concludes it would have been obvious to combine the references to provide a pressure for annealing the top electrode layer (p. 9). Applicants respectfully disagree.

Iizuka teaches away from the proposed combination. Iizuka discloses annealing "in a nitrogen atmosphere of 1 atmospheric pressure," (Col. 2, ll. 32-33), or "in a gas mixture atmosphere of oxygen concentration of 5% or below and nitrogen under 1 atmospheric pressure." (Col. 2, ll. 42-44). In other words, Iizuka discloses that in both embodiments, an anneal should be conducted *at atmospheric pressure, i.e.*, 760 Torr. Iizuka does not teach or suggest that the "annealing is performed at a pressure between 2 and 660 Torr," as recited in dependent claim 65. This is an additional reason for the allowance of dependent claim 65.

The Office Action also states that although Iizuka and Narwankar do *not* teach or suggest "a gas flow rate between .01-10 liters per second . . . [but] it would have been obvious" to obtain the specific range for the gas flow rate (pp. 9-10). The Office Action further asserts that no criticality has been established for the claimed range (p. 10). Applicants respectfully submit that the Office Action fails to set forth a

prima facie case of obviousness.

"To establish *prima facie* obviousness of a claimed invention, *all* the claim limitations must be taught or suggested by the prior art." M.P.E.P. § 2143.03 (emphasis added). Applicants respectfully submit that since neither Iizuka nor Narwankar discloses or suggests a gas flow rate, no evidence is required since the Office Action has failed to set forth a *prima facie* case of obviousness. *See* M.P.E.P. § 2144.05. As a result, neither Iizuka nor Narwankar, alone or in combination, renders Applicants' claimed gas flow rate obvious and the rejection should be withdrawn.

Claim 61 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,387,802 ("Marsh"). The rejection is respectfully traversed.

Claim 61 depends from claim 32 and should be similarly allowable with claim 32 for at least the reasons provided above with regard to claim 32, and on its own merits. Specifically, Iizuka does *not* disclose or suggest "annealing [a] dielectric layer with *a first anneal process* . . . forming a top electrode with a top conducting layer . . . and annealing the top electrode with *a second anneal process* using an oxidizing gas anneal, said oxidizing gas anneal performed *between 10 seconds to about 30 minutes*," as recited in claim 32 (emphasis added). Iizuka does not disclose, in either the first or second embodiment, a first and second anneal process or an anneal duration that is between 10 seconds to about 30 minutes.

Claim 97 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of Emesh. The rejection is respectfully traversed.

The cited references fail to teach or suggest the subject matter of amended independent claim 97. Specifically, Iizuka does not disclose a method of forming a capacitor comprising, *inter alia*, "forming a bottom electrode; forming a dielectric layer . . . forming a top electrode . . . and annealing said top electrode with an oxidizing gas anneal at a temperature *greater than 400°C*," as recited in claim 97 (emphasis added).

Iizuka discloses annealing "in a nitrogen atmosphere of 1 atmospheric pressure at temperature of *300 to 400 degrees C*," (Col. 2, ll. 32-34) (emphasis added), or "in a gas mixture atmosphere of oxygen concentration of 5% or below and nitrogen under 1 atmospheric pressure at temperature of *300 to 400 degrees C.*" (Col. 2, ll. 42-45) (emphasis added). Iizuka specifically teaches an annealing temperature of 300 to 400°C.

These facts are underscored by Iizuka's disclosure that the semiconductor production method is a "*low temperature anneal.*" (Col. 2, ll. 20-23) (emphasis added). As a result, there is *no* motivation to use a higher temperature than 400°C. Iizuka's methods are conducted to achieve a *low temperature* oxidizing anneal. As such, the cited references would not teach or suggest "annealing [a] top electrode with an oxidizing gas anneal at a temperature *greater than* 400°C," as recited in claim 97 (emphasis added).

Applicants also respectfully submit that the prior art of record does not teach or suggest the subject matter of newly added indepenent claim 98. The prior art of record does not disclose or suggest a method of forming a capacitor comprising, *inter alia*, "forming a bottom electrode; forming a dielectric layer . . . annealing the dielectric layer with a *first oxidizing gas anneal* for about 10 seconds to about 60 minutes, at a temperature from about 300 to about 800°C, and from about 1 to about 760 Torr; forming a top electrode over said annealed dielectric layer; and annealing said top electrode with *a second oxidizing gas anneal* for about 10 seconds to about 60 minutes, at a

temperature from about 300 to about 800°C, and from about 1 to about 760 Torr," as recited in claim 98.

As discussed above, at best, Iizuka discloses an oxidizing gas anneal *after* the entire structure is formed. Iizuka does not disclose or suggest that a first anneal is conducted on the dielectric layer, forming a top electrode on the *annealed dielectric layer*, and then performing a *second anneal* on the top electrode.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

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Respectfully submitted,

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